Through-Silicon Via (TSV)-induced Noise Characterization and Noise Mitigation using Coaxial TSVs

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Abstract—**Through-Silicon Via (TSV) is a critical interconnect element in 3D integration technology. TSVs introduce many new design challenges. In addition to competing with devices for real estate, TSVs can act as a major noise source throughout the substrate. We present in this paper a comprehensive study of TSV-induced noise as a function of several critical design and process parameters including substrate type, signal slew rate, TSV height, ILD thickness, and TSV-to-device and TSV-to-TSV spacing. We create a SPICE model for simulating TSV-to-device and TSV-to-TSV noise couplings in two different types of substrates: a lightly doped bulk substrate, and a lightly doped thin epitaxial layer on top of a heavily doped bulk. Our SPICE model provides small error when compared with a detailed Finite Element Analysis Method. Our findings show the importance of using a grounded backplane in reducing noise and how coaxial TSVs further mitigate TSV-induced noise.**

I. INTRODUCTION

Through-Silicon Vias (TSVs) connect multiple dies to form a 3D integrated circuit (IC). TSVs offer excellent electrical performance and packaging of various types of micro components (RF modules, sensors, etc.) directly on a CMOS chip. TSVs in a bulk CMOS technology are filled with a conductive metal, such as Copper or Tungsten, and surrounded by an isolation layer of dielectric or dielectric with a diffusion barrier. TSVs introduce many new design challenges. Due to the thin sidewall isolation layer (ILD) and the vertical extension throughout the substrate, electrical coupling and critical substrate noise can occur in neighboring active devices and TSVs. Substrate noise negatively impacts circuit performance [1] and threatens to cause logic failures.

Substrate noise in 2D ICs is well-studied and various experimental data and analytical models have been proposed to explore this phenomenon [2][3]. However, substrate noise due to TSVs in a 3D IC has not been adequately studied yet. Existing literature on TSV characterization falls under electrical (R & C) [4-7], thermal [8], or stress [9] analysis. Rousseau et al. present an early study of electrostatic impact of TSVs on CMOS transistors [10]. Their work introduces the potential issue of TSV-induced noise in devices. However they do not investigate the impact of various contributing factors and method for noise mitigation. Coaxial TSVs have been introduced to suppress undesirable substrate crosstalk for high frequency applications [11].

We present in this paper a comprehensive study of TSV-induced noise, in both devices and neighboring TSVs. Our work investigates three critical issues. First, we wish to identify and characterize critical process and design parameters that amplify TSV-induced noise. The resulting peak magnitude and location, as well as the noise distribution throughout the substrate are dependent on several process and design parameters. In particular, the substrate configurations (lightly doped (bulk) substrate *vs.* lightly doped epitaxial layer on top of heavily doped bulk) and the distance to the underling Gnd backplane (proportional to TSV height) affect the noise. ILD thickness also determines how a signal transition within a TSV impacts neighboring devices or TSVs. Understanding how critical circuit design parameters such as signal slew rate, and TSV-to-TSV (or TSV-to-Device) spacing impact noise allows establishing clear TSV design guidelines. Second, coaxial TSVs[11][12], novel TSV structures containing a second metal fill and a second ILD layer, provide additional signal shielding, and thus reduce noise, by connecting the outside metal layer to Vdd or Gnd. We therefore investigate how coaxial TSVs can reduce the "keep-away" zone required for noise reduction when compared to non-coaxial TSVs. Third, we must have confidence in our simulation and evaluation accuracy. We therefore use a distributed RC grid-like network to model substrate and circuit elements. To ensure our model's accuracy, we calibrate it against the results of Finite Element Analysis.

The total substrate area penalty for a TSV includes areas of the conductor, sidewall ILD, and any keep-away zone required for noise reduction. Therefore, effective and area efficient isolation techniques are desirable in noise critical applications. While the maturity of the process flow for TSV technologies is still in active research, our study and results demonstrate the importance of early investigation for potential applications and circuit design implications.

The rest of the paper is organized as follows: we describe the substrate configurations with TSVs and our SPICE model in section II. We present the key results and observations from the TSV-to-device and TSV-to-TSV noise analyses in sections III and IV, respectively. In section V, we analyze noise mitigation using coaxial TSV. Finally, we provide the conclusion in section VI.

II. PROCESS AND DESIGN PARAMETERS FOR SPICE MODEL

Our setup for noise analysis, in a thinned substrate with TSVs, comprises of two substrate configurations. The first

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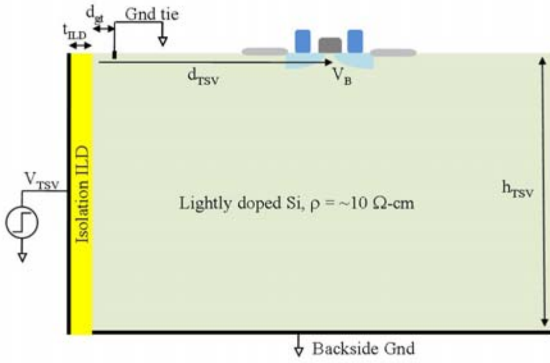

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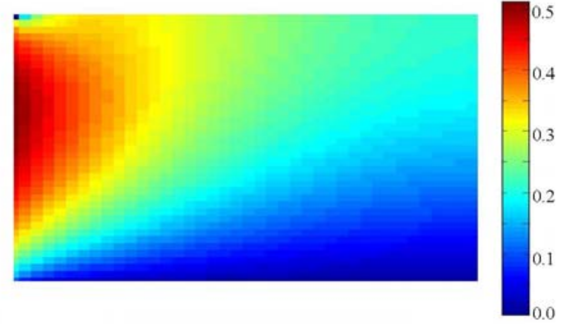

(b)

Fig. 1 (a) Cross-section view for High-R substrate (b) Noise distribution in volts for a set of process and design parameters (V_{TSV}=1V square wave, h_{TSV}=20µm, t_{ILD}=1µm, d_{gt}=0µm, signal transition time=50ps, and backside is grounded)

configuration, illustrated in Fig. 1-a, is the lightly doped (high resistive) substrate (High-R substrate) with a uniform resistivity of 10Ω-cm. This type of substrate is used to fabricate the low cost, low performance devices like memory [13]. The second configuration is the heavily doped bulk with lightly doped epitaxial layer (EPI substrate). We assume that the epitaxial layer spans the top 4µm of the substrate and has a resistivity of 10Ω-cm and rest of the bulk substrate has resistivity of 10mΩ-cm. This type of configuration is mostly used to fabricate the high performance chips like processor [13].

A signal transition in the TSV is modeled as a square wave voltage source V_{TSV}. The sidewall isolation ILD and the Si substrate are modeled as an RC grid like network. The size of an individual grid element or equivalently the resolution of the grid is an important factor that impacts the accuracy of the noise analysis. Therefore, we evaluated the accuracy of the SPICE-based model for appropriate grid size. We performed electrostatic analysis with multiple grid sizes (1µm, 0.5µm, 0.2µm, and 0.1µm) and compared the results with commercially available finite element method (FEM) solver from Ansoft[1]. We observe that 0.5µm grid size has the smallest error. Maximum and average error in V_B was 4.5% and 2.05% respectively and for substrate noise these values were 4% and 1.67% respectively as compared to the FEM results.

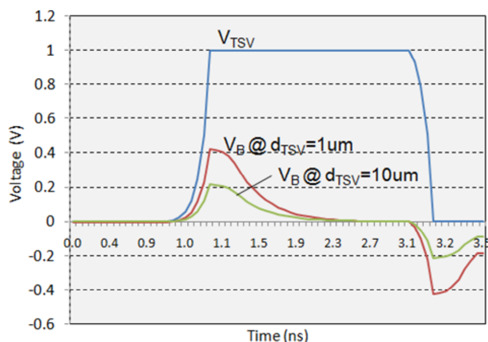

Fig. 2. Body voltage at different TSV distances, d_{TSV}, for V_{TSV} of a square wave input.

[1] Ansoft LLC http://www.ansoft.com/

Although FEM-based analysis provides more accuracy than the SPICE-based model, it's the FEM long runtime that makes it unsuitable for comprehensive characterization especially when multiple parameters are involved. Fig. 1-a shows all the parameters of interest in our noise analysis: sidewall ILD thickness t_{ILD}, distance to substrate ground (Gnd) tie d_{gt}, distance to device body d_{TSV}, and TSV height h_{TSV}.

Neighboring substrate Gnd tie where d_{gt}=0µm is the conventional form of noise isolation, and hence, is considered in our scheme. We developed automated scripts to create circuits, conduct SPICE simulation, and process results for all the other parameter variations. Transient SPICE simulation is performed to estimate coupling noise over time across the substrate. Fig. 1-b shows the maximum transient voltage induced in the substrate when a square-wave input is applied as V_{TSV}. This figure shows that the noise problem is more prominent inside the substrate (in close vicinity of TSV) than at the top surface where the devices are fabricated. Fig. 2 illustrates the transient noise in body voltage V_B for a square wave input of 1V peak for V_{TSV}.

Fig. 1-a also shows a backside Gnd plane attached to the substrate in our configurations. Although placing the substrate on a grounded plane can be found in selected 2D packaging for noise reduction [14], backside Gnd plane for each layer in 3D IC is not yet established. We first conducted transient noise simulation both with and without the backside Gnd. Fig. 3 plots the peak body voltage, V_B, at varying distance from TSV, d_{TSV}, when V_{TSV} switches from 0V to 1V. We present our findings from Fig. 3:

- Peak value of V_B in either High-R or EPI substrate without the backside Gnd plane is very high, close the transition voltage. This is due to the coupling noise i.e. coupling and charge sharing in the substrate, and lack of abundant Gnd connections for charge collection.
- The backside Gnd plane is very effective in reducing the peak V_B. Maximum noise in EPI substrate is reduced by 75% whereas the same is reduced by 30.5% in High-R substrate.
- With the backside Gnd plane, EPI substrate has more localized noise with peak V_B of 25% of Vdd and V_B

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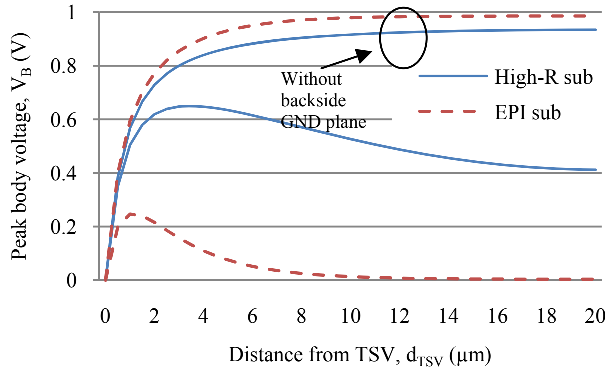


Fig 3. Peak body voltage for substrate with and without backside Gnd plane.

falling to less than 10% of Vdd at distance of 4µm. Even with the Gnd backplane, High-R substrate noise is significantly large with a peak V_B of 65% of Vdd, and not so localized to TSV neighboring area. The substrate Gnd tie next to TSV reduces noise only in the immediate neighborhood area. Based on the above analysis, we conclude that the Gnd backplane is essential for noise reduction in either type of substrates, and thus, include it in rest of the analysis to characterize TSV-to-device and TSV-to-TSV noise.

III. TSV-TO-DEVICE NOISE CHARACTERIZATION

A voltage transition in the TSV affects nearby substrate voltage, changing the body voltage (V_B) of the device. Although the duration (rise/fall time of the TSV signal) of this noise is small (as shown is Fig. 2), it can result in significant performance impact for both analog and digital circuits. For analog circuits the peak magnitude should be within the noise tolerance margin of the device, but for digital device, timing of the peak is more important.

In this section, we characterize V_B variations due to signal transition in a nearby TSV. We model the substrate as RC network as described in the previous section and study the voltage variations within the 20µm distance of the TSV. Since devices are fabricated at upper part of the silicon, we only consider noise at the surface of the substrate for TSV-to-device noise characterization. Followings are the details of each of the studies with critical design and process parameters:

A. Signal Slew Rate

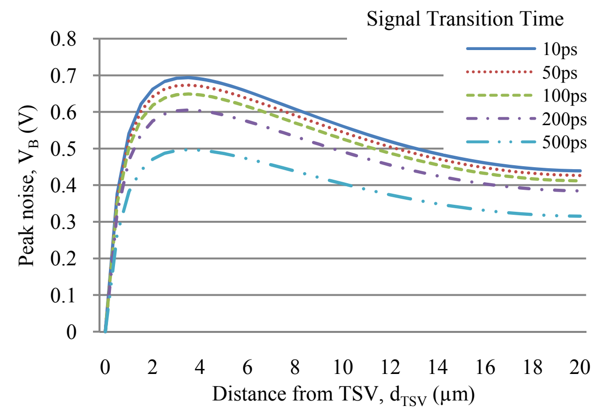
Signal slew rate is an important circuit design parameter related to circuit power and performance. We fix the Vdd to 1V and change the signal transition (rise/fall) time to vary the slew rate. We use different values for signal transition time between 10ps and 500ps, and observe peak noise in V_B as shown in Fig. 4 for both substrate configurations. The TSV sidewall ILD thickness, t_{ILD}, is fixed at 50nm, while the TSV height, h_{TSV}, is fixed at 20µm. We make the following observations:

- As we increase the transition time of the signal in the aggressor TSV, V_B is reduced at all distances in the substrate.
- The location of peak noise is independent of the slew rate in the High-R as well as EPI substrates. Peak noise always occurs at d_{TSV} of 3.5µm and 1µm in the High-R and EPI substrates, respectively. This has an interesting implication in TSV-to-device spacing (keep-away zone) design rule development: any spacing rule to avoid peak V_B is independent of the signal transition time.
- Controlling the TSV signal slew rate is more effective in mitigating TSV-to-device noise in EPI substrate than in High-R substrate. In the High-R substrate, a 28% decrease in peak noise is observed for a 50 fold (10ps to 500ps) increase in signal transition time. However, a 70% reduction is noise is possible for the same signal transition range in the EPI substrate.

B. Sidewall ILD Thickness

The TSV sidewall ILD thickness is the first critical process parameter that affects TSV-to-device noise. The coupling capacitance is inversely related to the ILD thickness. We use various ILD thickness values ranging from 50nm to 1.5µm, and observe the body voltage V_B as shown in Fig. 5. The TSV signal transition time is fixed at 100ps while the TSV height, h_{TSV}, is fixed at 20µm. Here are some key observations:

- Similar to the signal slew rate, ILD thickness does not have any impact on the locality of the peak V_B. The location of peak V_B remains the same at d_{TSV} of 3.5µm and 1µm for the two substrate configurations as shown in Fig. 5.
- The effectiveness in TSV-to-device noise mitigation via



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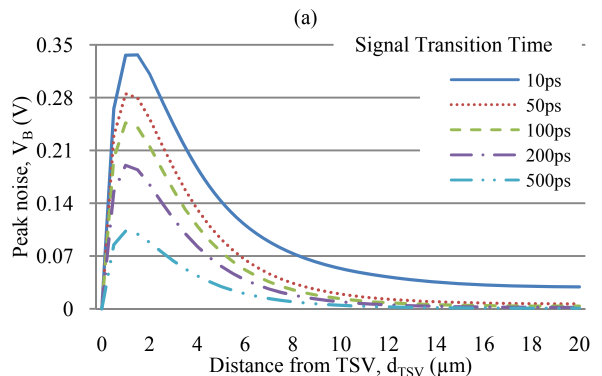

Fig 4. TSV-to-device noise distribution for different slew rates. (a) High-R substrate (b) EPI substrate

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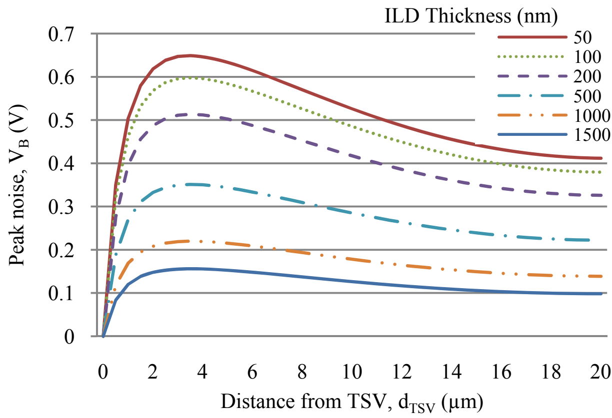

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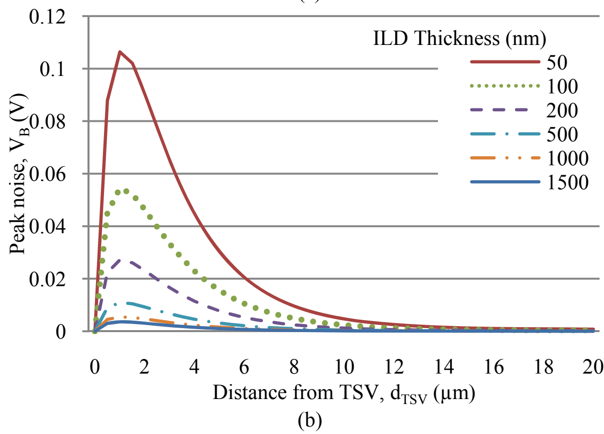

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Fig 5. TSV-to-device noise distribution for different ILD thicknesses. (a) High-R substrate (b) EPI substrate

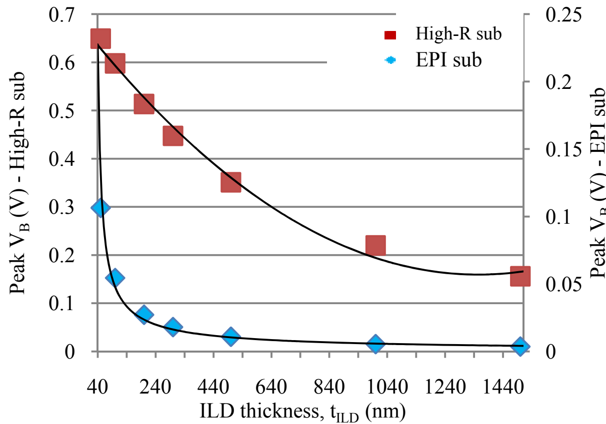


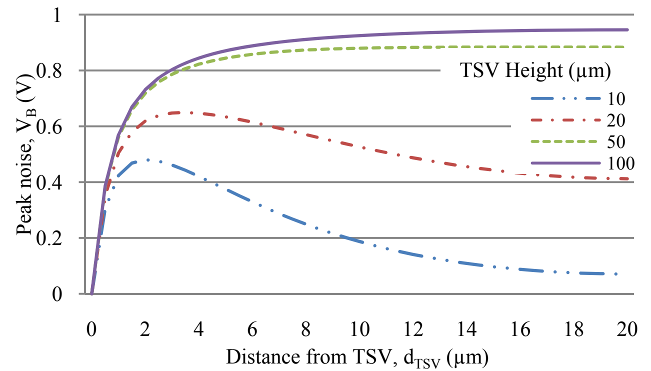
Fig. 6. Peak body voltage vs. ILD thickness in High-R and EPI substrates.

controlling the ILD thickness is illustrated in the peak V_B vs. ILD thickness plot shown in Fig. 6. Peak noise reduction with increasing t_{ILD} saturates after an ILD thickness that is different depending on the substrate type. In High-R substrate, a high ILD thickness (larger than 1µm) is desirable to optimally reduce TSV-to-device noise. On the other hand, noise reduction saturates as early as 250nm ILD thickness in EPI substrate. This observation suggests that higher values of ILD thickness will be required to implement a 3D system using High-R substrate than the same for EPI substrate.

C. *TSV Height*

Another critical process parameter for TSV-to-device noise is the TSV height which equivalently corresponds to the die thickness. Die/wafer thickness is a constraint in the 3D IC process due to TSV aspect ratio and thinned wafer handling limitations. In this experiment, we vary the TSV height, ranging from 10µm to 200µm, for both substrate configurations. We analyze V_B for different TSV heights. The TSV signal transition time is fixed at 100ps, while the TSV sidewall ILD thickness, t_{ILD}, is fixed at 50nm. The results are presented in Fig. 7. Here are some key observations:

- Unlike the previous cases, we see TSV height significantly affects the locality of the peak V_B as evident in Fig. 7. In addition to increasing the peak noise amplitude, increasing



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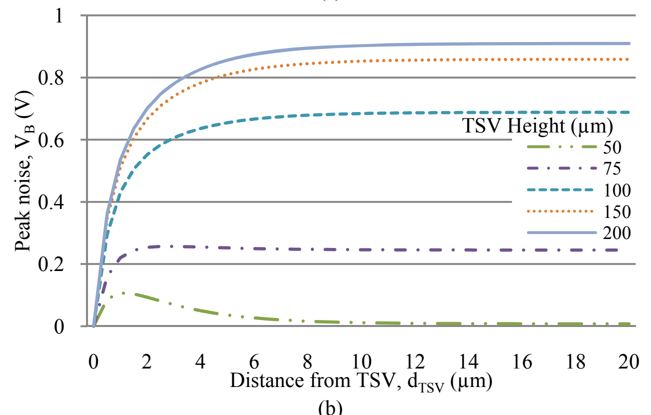

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Fig 7. TSV-to-device noise distribution for different TSV heights. (a) High-R substrate (b) EPI substrate

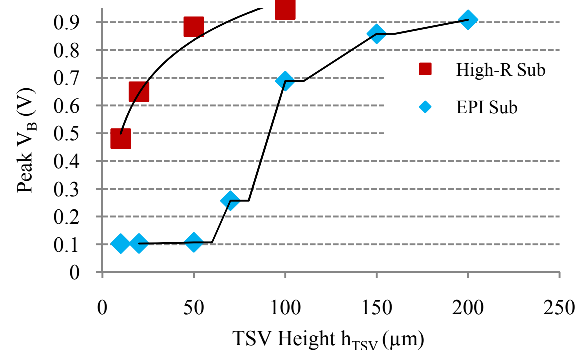

Fig. 8. Peak body voltage vs. TSV height in High-R and EPI substrates.

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the TSV height increases the affected substrate area.

- The TSV-to-device noise or substrate noise can be added as a design constraint in determining TSV height. We performed such an analysis, and the results are shown in Fig. 8. The results provide insight into the impact of TSV height on peak noise. In High-R substrate, substrate noise increases monotonically with TSV height. At the smallest height (10µm in our analysis) the noise is significant (50% of Vdd). On the other hand, peak noise vs. TSV height in EPI substrate shows two distinct trends. There is no significant reduction in TSV-to-device noise when the TSV height is below 50µm. Peak TSV-to-device noise remains at 10% of Vdd. For larger heights (>50µm) TSV-to-device noise increases monotonically. The exact value of such TSV height threshold would vary with different material properties and the depth of epitaxial layer. However, the general observation that there exists such a TSV height threshold for the height of any of the substrate configurations is still applicable.

IV. TSV-TO-TSV NOISE CHARACTERIZATION

In addition to nearby devices, TSV noise impacts nearby TSVs as well. While power supply TSVs are expected to be placed in a regular fashion, signal TSVs can be grouped into a bus where smaller TSV spacing is desirable for performance or area savings. To study TSV-to-TSV coupling noise, one of the TSV is denoted as the aggressor and the other TSV, driven to Gnd, is denoted as the victim. We assume that the victim TSV is pulled to Gnd using moderately large drive strength (W/L ratio of 20) in 20nm node from ITRS[2]. We report the peak transient noise at the victim TSV when a square wave voltage source is applied to the aggressor TSV. A SPICE-based model is generated using RC elements similar to TSV-to-device noise analysis. The backside Gnd plane and a substrate Gnd tie right next to each TSV are also employed using the general approach of modeling setup according to Section II. The parameters of interest for TSV-to-TSV noise characterizations are TSV spacing, sidewall ILD thickness, and TSV height.

Fig. 9 shows the peak noise at the victim TSV for different values of TSV-to-TSV spacing considering a range of TSV heights. Here, the TSV signal transition time is fixed at 100ps, while the TSV sidewall ILD thickness, t_{ILD}, is fixed at 50nm. As expected, the peak noise at the victim TSV shows a saturation trend with increasing TSV spacing. Furthermore, the larger the TSV height, the longer the TSV spacing to achieve that noise saturation. Therefore, smaller TSV heights are needed to enable routing signal TSVs in a smaller region.

When TSVs are spaced at their noise saturated distance, for any given TSV-to-TSV spacing, peak TSV noise is linearly dependent on TSV height in High-R substrate. The EPI substrate, on the other hand, shows that there is no significant TSV-to-TSV noise for TSV height smaller than 50µm. This characteristic, also seen in TSV-to-device noise in section III, is due to the presence of thin high-R layer (4µm in our configuration) over a thicker low-R bulk substrate and is dependent on the ratio of their thicknesses after substrate thinning. Reducing the TSV height in EPI substrate, beyond a specific value, does not have similar benefit in noise reduction as in High-R substrate. Therefore, TSV height or equivalently substrate thickness can be lower in high-R substrate than that of EPI substrate. Interestingly, the observed trend from noise characteristics is in agreement with TSV heights reported in the ITRS[2]. ITRS data suggests that for low performance 3D ICs (typically done in High-R substrate), die thickness is much smaller compared to that for high performance chips (typically done in EPI substrate).

Next, we analyze the impact of sidewall ILD thickness on TSV-to-TSV noise. Fig. 10 shows peak TSV noise over a range of ILD thickness in both configurations. Here, the TSV height is fixed at 100µm. Similar to our observations in TSV-to-device noise characteristics, a larger ILD thickness (greater

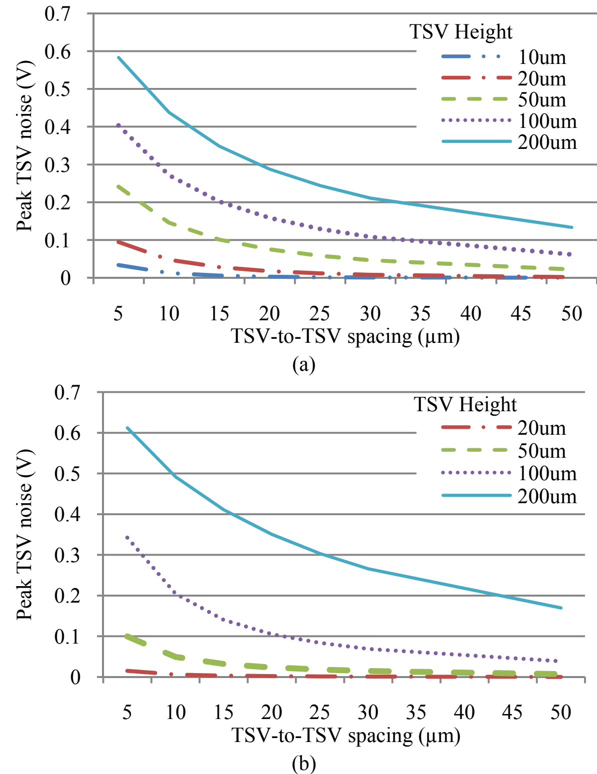

Fig 9. Peak TSV noise vs. TSV spacing for different TSV heights. (a) High-R substrate (b) EPI substrate

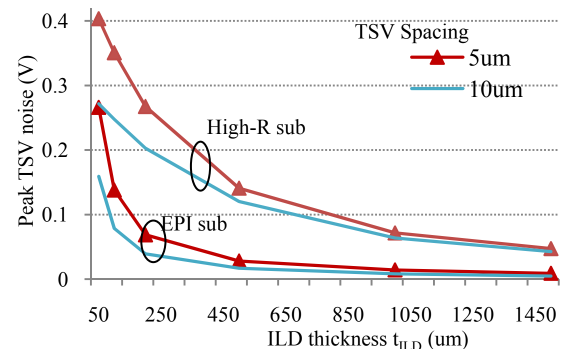

Fig. 10. Peak TSV noise vs. TSV sidewall ILD thickness in High-R and EPI substrates.

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[2] http://www.itrs.net/Links/2008ITRS/Home2008.htm

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than 1μm) in High-R substrate is required compared to that (approximately 0.5μm) in EPI substrate to best reduce TSV-to-TSV noise.

V. Noise Mitigation using Coaxial TSV

The analyses presented in the previous sections show that signal TSVs can inject significant noise in the substrate. The required high sidewall ILD thickness and any additional "keep away" zone contribute to a high substrate area penalty in noise critical applications. Coaxial TSVs can be employed as a noise mitigating solution with a smaller area penalty than traditional TSVs. A coaxial TSV, illustrated in Fig. 11, contains a second metal fill (outer metal) surrounding the first sidewall ILD, and then another layer of ILD surrounding the outer metal. Coaxial TSVs, presented earlier in [11][12], can eliminate the substrate noise by grounding the outer metal layer while the inner metal layer is used for signal transmission.

While the details of coaxial TSV fabrication process is out of the scope of this work and is under active investigation, here we analyze the substrate noise reduction using a coaxial TSV. Based on our analyses and ITRS reported data on TSVs, we choose a representative set of process and manufacturing parameters presented in Table I for TSV-induced noise estimation. We investigate TSV-induced noise distribution for three setups: without a backside Gnd plane, with a backside Gnd plane, and using a coaxial TSV, in each of the two substrate configurations. Results of TSV-induced noise in both devices and neighboring TSVs are reported in Table I. We also

TABLE I
REPRESENTATIVE TSV-INDUCED NOISE IN DIFFERENT SUBSTRATE CONFIGURATIONS

	Substrate Configurations	
	High-R	EPI
Process/Manufacturing Parameters		
TSV Height (minimum height as per ITRS data)	20μm	50μm
Sidewall ILD Thickness (optimal thickness as per our analyses)	1.0μm	0.5μm
Design Parameter		
Signal Transition Time	50ps	50ps
Supply voltage Vdd	1V	1V
TSV-induced Noise Results (without backside Gnd plane)		
Peak body voltage, V_B	0.74V @20μm	0.97V @20μm
Keep-away zone for V_B < 20% of supply	>20μm	>20μm
Peak TSV noise (@5μm spacing)	0.01V	0.08V
TSV-induced Noise Results (with backside Gnd plane)		
Peak body voltage, V_B	0.33V @3.5μm	0.10V @1μm
Keep-away zone for V_B < 20% of supply	19.5μm	0μm
Peak TSV noise (@5μm spacing)	0.02V	0.007V
TSV-induced Noise Results (Coaxial TSV)		
Peak body voltage, V_B	0.01V @ 1μm	0.01V @ 1μm
Keep-away zone for V_B < 20% of supply	0μm	0μm
Peak TSV noise (@5μm spacing)	<0.01V	<0.01V

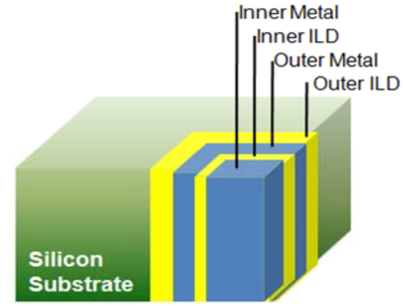

Fig 11. Schematic illustration of a coxial TSV in a Si substrate using a cross-section view.

report device keep-away zone defined as the device distance from TSV for peak body voltage less than 20% of Vdd supply. We don't employ any backside Gnd plane or neighboring substrate tie in the coaxial TSV analysis setup. Results presented in Table I show that shielding of a signal TSV to form a coaxial TSV has a significant impact on the noise reduction in the substrate. When utilizing the coaxial TSVs, a 33x and 10x reduction in TSV-to-device noise is possible over the High-R and EPI substrate configurations with the Gnd backplane.

VI. Conclusion

We presented a comprehensive study for TSV-induced noise characterization in High-R and EPI substrates as a function of several critical design and process parameters including signal slew rate, TSV height, ILD thickness, and TSV-to-device and TSV-to-TSV spacing. One key finding is the need for aggressive shielding using either a backside Gnd plane or advanced TSV technologies such as coaxial TSVs. It is important to note that shielding utilizing coaxial TSVs can perform double-duty as an effective mean for enhancing 3D power delivery [15]. Another finding is that an EPI substrate quells noise issues more aggressively than a High-R substrate. The resulting keep-away area is thus smaller and allows packing signals and devices closer to signal TSVs. We also found that TSV height is a critical parameter in determining the location of peak noise and that variations of signal slew rate and ILD thickness do not affect the location of peak noise. Moreover, the TSV height has minimal impact on noise magnitude once the height is reduced to less than 50 μm in EPI substrate. Our presented work thus provides valuable insight into creating guidelines for TSV-to-TSV and TSV-to-device spacing, and calls for macro-models for analytically understanding and characterizing the impact and sensitivity of process and design parameters on TSV-induced noise in 3D designs.

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